**IN THE CLAIMS**

Please cancel claims 1 and 3-5 without prejudice or disclaimer as to their subject matter by this amendment:

Claims 1-5 (Canceled)

6. (Previously Presented) A flat panel display, comprising:

a thin film transistor comprising source and drain electrodes, arranged on an insulation substrate;

a gate insulation film arranged on the insulation substrate and on the thin film transistor, the gate insulation film being perforated by first and second contact holes exposing the source and drain electrodes respectively;

a gate electrode, a lower electrode of a capacitor and gate lines being arranged on the gate insulation film;

an interlayer insulation film arranged on the gate electrode, the lower electrode of the capacitor and the gate lines;

an upper electrode of the capacitor and data lines being arranged on the interlayer insulation film;

a passivation film arranged on the upper electrode of the capacitor and on the data lines

a pixel electrode arranged on the passivation film and electrically connected to one of the source and drain electrodes through one of the first and second contact holes; and

a power supply layer also arranged on the passivation film and electrically connected to the other one of the source and drain electrodes through the other one of the first and second contact holes.

7. (Previously Presented) The flat panel display of claim 6, the power supply layer and pixel electrode being comprised of the same material.

8. (Previously Presented) The flat panel display of claim 6, the power supply layer and pixel electrode being comprised of a material having both a low resistivity and a high reflectivity.

9. (Previously Presented) The flat panel display of claim 7, wherein the pixel electrode and the power supply layer being comprised of a single film of a material selected from the group consisting of Au, Pt, Ni, Cr, a laminated Ni/Al/Ni film, a laminated Ag/ITO film and a laminated Al/ITO film.

10. (Previously Presented) A flat panel display, comprising:

an insulation substrate divided into a plurality of pixel regions, each of said pixel regions being defined by a crossing of a gate line and a data line, the insulation substrate comprising a plurality of thin film transistors, each thin film transistor being arranged in corresponding ones of said plurality of pixel regions;

a first insulation film arranged on the substrate and on the plurality of thin film transistors;

a gate electrode, gate lines and data lines arranged on the first insulation film;

a second insulation film arranged on the gate electrode, the gate lines and the data lines;

a plurality of pixel electrodes arranged on the second insulation film and being electrically connected to corresponding ones of said plurality of thin film transistors in corresponding ones of said plurality of pixel regions; and

a power supply layer also arranged on the second insulation film, the power supply layer being electrically separated from the plurality of pixel electrodes, said

power supply layer being electrically connected to each of the plurality of thin film transistors and supplying power to each of the plurality of thin film transistors.

11. (Previously Presented) The flat panel display of claim 10,an entirety of the power supply layer being separated from an entirety of each of the gate lines and the data lines by the second insulation film.

12. (Original) The flat panel display of claim 10, the power supply layer being formed in a line shape in which the power supply layer is arranged between corresponding ones of said plurality of pixel electrodes, said power supply layer being arranged in one of a row or a column.

13. (Original) The flat panel display of claim 10, the power supply layer having a surface electrode shape in which the power supply layer is formed on a whole surface of the substrate and being electrically separated from each of the plurality of pixel electrodes.

Claims 14-20 (Canceled)

21. (Previously Presented) The flat panel display of claim 6, an entirety of the power supply layer being separated from an entirety of the data lines by the passivation film.

22. (Previously Presented) The flat panel display of claim 21, an entirety of the power supply layer being separated from an entirety of the gate lines by the passivation film and the interlayer insulation film.

23. (Previously Presented) The flat panel display of claim 10, wherein the power supply layer surrounds each of said plurality of pixel electrodes, the power supply layer comprises a plurality of electrodes extending in a first direction and a plurality of electrodes extending in a second direction intersecting the electrodes extending in the first direction.